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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,260	08/16/2000	Joseph B. Tompkins	9215/020	4626

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EXAMINER

NGUYEN, ALAN V

ART UNIT	PAPER NUMBER
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2662

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/640,260

Applicant(s)

TOMPKINS ET AL.

Examiner

Alan Nguyen

Art Unit

2662

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 August 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 7, 10, and 13 are objected to because of the following informalities:

Claim 8, line 9, "classes" should read --classes.--.

Claim 9, line 12, "classes" should read --classes.--.

Claim 25, line 9, "classes" should read --classes.--.

Claim 26, line 12, "classes" should read --classes.--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 and 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al (US 6,504,846), herein Yu.

Regarding **claims 1 and 18**, Yu discloses an integrated circuit ("**Structure that is on-chip, column 11 lines 60-61**") that processes communication packets ("**...enable communication of data packets", column 4, lines 57-58**), the integrated circuit comprising:

a pointer cache (**figure 2, element 64**) configured to store pointers that correspond to external buffers that are external to the integrated circuit and configured to store the communication packets (**"...outputs the received data packet to the external memory interface 44 for storage in the external memory 36 at the location specified by the frame pointer", column 6, lines 56-59**); and

control logic configured to allocate the external buffers as the corresponding pointers are read from the pointer cache (**"The queuing logic uses the fetched frame pointers to store received data to the external memory", column 8, lines 28-29; column 8, lines 50-55 further describes a scheduler that receives write requests from the queuing logic and generates a "grant" to initiate a transfer of the data to the memory slot.**) and de-allocate the external buffers as the corresponding pointers are written back to the pointer cache (**Column 14, lines 19-29 states that the reclaim control logic ensures that all frame buffers used to store a received data frame are released by walking the linked list of frame buffers. As the linked list of the frame buffer is walked, the reclaim control logic inputs the free buffer pointer associated with each frame buffer into the free buffer queue**).

Regarding **claims 2 and 19**, with the features in parent claim 1 addressed above, Yu discloses wherein the control logic is configured to track a number of the pointers to the de-allocated external buffer (**"When frame pointers are written into an empty reclaim queue, they pass from the reclaim queue write side to the reclaim queue read side until the read side is full", column 13, lines 65-67**).

Regarding **claims 3 and 20**, with the features in parent claim 1 addressed

above, Yu discloses wherein the control logic is configured to transfer additional pointers to the pointer cache if a number of the pointers to the de-allocated buffers reach a minimum threshold (***"The ordering of the frame pointers input to the reclaim queue write side 612 may be maintained such that when space clears in the reclaim queue read side, frame pointers are moved from the reclaim queue overflow area to the reclaim queue read side", column 14, lines 13-17***).

Regarding **claims 4 and 21**, with the features in parent claim 1 addressed above, Yu discloses wherein the control logic is configured to transfer an excess portion of the pointers from the pointer cache if a number of the pointers to the de-allocated buffers reach a maximum threshold (***Column 13, lines 65-67 and column 14, lines 1-3 state that when the reclaim queue read side is full, additional frame pointers written to the reclaim queue write side are placed into the reclaim queue overflow are in external memory***).

Regarding **claims 5 and 22**, with the features in parent claim 1 addressed above, Yu discloses wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold (***Inherent, column 14, lines 13-17 states that frame pointers are moved from the overflow area to the queue read side when it reaches a certain level. A threshold signal must be present to notify the control logic of the situation***).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Sistare et al (US 6,601,089), herein Sistare.

Regarding **claims 6 and 23** Yu discloses the use of a buffer pool ("The buffer pointer obtained from the free buffer pool", column 8, lines 59-60).

Yu fails to disclose wherein the external buffers are distributed among at least two pools.

Sistare teaches the use of multiple buffer pools (**Column 5, lines 16-20 discusses how each device or process has its own buffer pool. This allows the device or process to have exclusive ownership and control over the buffers in its buffer pool**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for Yu to utilize multiple pools for the buffers, the reason being that pools are helpful when the external buffers are located in separate memory, so each device may have its own independently managed pool, as taught by Sistare.

4. Claims 7-17 and 24-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Janoska et al (US 6,539,024), herein Janoska.

Regarding **claims 7, 14-17, 24, and 31-34**, Yu discloses the use of external

buffers and pointers that point to the external buffers (***"The unit outputs the received data packetto the external memory interface for storage in the external memory at the location specified by the pointer", colmun 6, lines 54-59***). Yu also discloses in column 7, lines 20-22 a use of a class identifying whether the frame is high or low priority.

Yu fails to show wherein the external buffers and the pointers to the external buffers are distributed among a plurality of classes.

Janoska teaches the use of having received data cells being put into different classes based on their type of service in the communication network (***"The potential classes of service include constant bit rate (CBR), variable bit rate (VBR), available bit rate (ABR), and unspecified bit rate (UBR), column 3, lines 54-61***).

It would have been obvious to one having ordinary skill in the art at the time the invention was made for Yu to utilize different classes for each of the different traffic stream, for example, CBR, VBR, ABR, and UBR. The motivation is a trend for the packet processors to provide certain traffic streams a greater access to external buffers depending on its type, since each of the different categories provide a different quality of service that may be desirable to various users of the communications network, as taught by Janoska.

Regarding **claims 8 and 25**, with the features in parent claim 7 addressed above, Yu, as modified, discloses wherein the control logic is configured to track a number of the pointers to the de-allocated external buffers for at least one of the classes (***"When frame pointers are written into an empty reclaim queue , they pass from***

the reclaim queue write side to the reclaim queue read side until the read side is full", column 13, lines 65-67).

Regarding **claims 9 and 26**, with the features in parent claim 7 addressed above, Yu, as modified, discloses wherein the control logic is configured to track a number of the pointers to the allocated external buffer for at least one of the classes (***"Buffer pointers written into the free buffer queue pass from the free buffer queue write side to the free buffer queue read side until the read side is full", column 14, lines 43-45).***

Regarding **claims 10, 11, 27, and 28**, with the features in parent claim 7 addressed above, Yu further fails to teach wherein the control logic is configured to borrow or re-distribute at least some of the pointers from a first one of the classes for use by a second one of the classes (Janoska teaches in column 6, lines 29-37 and figure 5, element 120 a shared portion that is used by all of the logical queues containing various traffic streams. The shared portion provides a large buffering resource that may be used by any one of the logical queues to store data that exceed the reserved capacity of the logical queue. It would have been obvious to one having ordinary skill in the art at the time the invention was made for Yu to utilize a shared resource scheme that can either borrow or lend pointers since it encourages more efficient use of buffering resources that is available for the traffic streams).

Regarding **claims 12 and 29**, with the features in parent claim 7 addressed above, Yu, as modified, discloses wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers in one of the

classes reaches a minimum threshold (*Inherent, column 14, lines 13-17 states that frame pointers are moved from the overflow area to the queue read side when it reaches a predetermined level. A threshold signal must be present to notify the control logic of that situation*).

Regarding **claims 13 and 30**, with the features in parent claim 7 addressed above, Yu, as modified, discloses wherein the control logic is configured to track a number of the pointers distributed to one of the classes ("*Buffer pointers written into the free buffer queue pass from the free buffer queue write side to the free buffer queue read side until the read side is full*", column 14, lines 43-45).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent is cited to show the state of the art with respect to buffer allocation and de-allocation

US Patent (6,526,499) to Palanca et al

US Patent (6,341,325) to Franaszek et al

US Patent (5,978,898) to Hathaway et al

US Patent (5,689,707) to Donnelly

US Patent (5,151,895) to Vacon et al

The following patent is cited to show the state of the art with respect to using external memory for storing buffers

US Patent (6,487,212) to Erimli et al

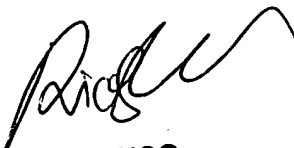
US Patent (6,175,902) to Runaldue et al

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan Nguyen whose telephone number is 703-305-0369. The examiner can normally be reached on 8am-5pm ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 703-305-4798. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

AVN
November 13, 2003


RICKY NGO
PRIMARY EXAMINER